

| REVISIONS | | | |
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| LTR | DESCRIPTION | DATE | APPROVED |
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Prepared in accordance with ASME Y14.24

Vendor item drawing

| | | | | | | | | | | | | | | | | | | | | |
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| REV STATUS OF PAGES | REV | | | | | | | | | | | | | | | | | | | |
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|--|--------------------------------------|---|------------------------------------|
| PMIC N/A | PREPARED BY Phu H. Nguyen | DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil/ | |
| Original date of drawing YY MM DD 12-11-08 | CHECKED BY Phu H. Nguyen | TITLE MICROCIRCUIT, LINEAR, LC ² MOS, QUAD SPST SWITCHES, MONOLITHIC SILICON | |
| | APPROVED BY Thomas M. Hess | | |
| | SIZE A | CODE IDENT. NO. 16236 | DWG NO. V62/12638 |
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance LC²MOS, quad SPST switches microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

| | | | | |
|------------------|---|----------------------------|-----------------------------|----------------------------|
| <u>V62/12638</u> | - | <u>01</u> | <u>X</u> | <u>E</u> |
| Drawing number | | Device type (See 1.2.1) | Case outline (See 1.2.2) | Lead finish (See 1.2.3) |

1.2.1 Device type(s).

| <u>Device type</u> | <u>Generic</u> | <u>Circuit function</u> |
|--------------------|----------------|--|
| 01 | ADG201A-EP | LC ² MOS quad SPST switches |

1.2.2 Case outline(s). The case outlines are as specified herein.

| <u>Outline letter</u> | <u>Number of pins</u> | <u>JEDEC PUB 95</u> | <u>Package style</u> |
|-----------------------|-----------------------|---------------------|--------------------------------|
| X | 16 | JEDEC MS-012-AC | Standard Small Outline Package |

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

| <u>Finish designator</u> | <u>Material</u> |
|--------------------------|----------------------|
| A | Hot solder dip |
| B | Tin-lead plate |
| C | Gold plate |
| D | Palladium |
| E | Gold flash palladium |
| Z | Other |

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1.3 Absolute maximum ratings. 1/

| | |
|--|---|
| V _{DD} to V _{SS} | 44.0 V |
| V _{DD} to GND | 25.0 V |
| V _{SS} to GND | -25.0 V |
| Analog inputs | V _{SS} – 0.3 V to V _{DD} + 0.3 V 2/ |
| Digital inputs | V _{SS} – 2 V to V _{DD} + 2 V or 20 mA (whichever occurs first) 2/ |
| Pulsed current, S or D | 70 mA (pulsed at 1 ms, 10% duty cycle maximum) |
| Continuous current, S or D | 30 mA |
| Operating temperature rang | -55°C to +125°C |
| Storage temperature range | -65°C to 150°C |
| Power dissipation: | |
| Up to +75°C | 470 mW |
| Derates above +75°C by | 6 mW/°C |
| Lead soldering: | |
| Reflow, Peak temperature | 26(+0/-5)°C |
| Time at Peak temperature | 20 sec to 40 sec |

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3 and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.5 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

- 3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.
- 3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.
- 3.5.3 Terminal function. The terminal function shall be as shown in figure 3.
- 3.5.4 Truth table. The truth table shall be as shown in figure 4.
- 3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.
- 3.5.6 On resistance. The on resistance shall be as shown in figure 6.
- 3.5.7 Off leakage. The off leakage shall be as shown in figure 7.
- 3.5.8 On leakage. The on leakage shall be as shown in figure 8.
- 3.5.9 Switching time. The switching time shall be as shown in figure 9.
- 3.5.10 Charge injection. The charge injection shall be as shown in figure 10.
- 3.5.11 Off isolation. The off isolation shall be as shown in figure 11.
- 3.5.12 Channel to channel crosstalk. The channel to channel crosstalk 12.

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TABLE I. Electrical performance characteristics. 1/

| Test | Symbol | Test conditions 2/ | Limits | | | | Unit |
|--------------------------------|-------------|--|----------|------|----------------|------|------|
| | | | 25°C | | -55°C to +125° | | |
| | | | Min | Max | Min | Max | |
| DUAL SUPPLY | | | | | | | |
| Analog switch | | | | | | | |
| Analog signal range | | | ±15 | | ±15 | | V |
| On Resistance (RON) | RON | -10 V ≤ VS ≤ +10 V, IDS = 1 mA; see FIGURE 6 | 60 TYP | | | 145 | Ω |
| RON vs VD(Vs) | | | 20 TYP | | | | % |
| RON Drift | | | 0.5 TYP | | | | %/°C |
| RON Match | | VS = 0 V, IDS = 1 mA | 5 TYP | | | | % |
| Leakage currents | | | | | | | |
| Source off leakage | IS (Off) | VD = ±14 V, VS = ∓14 V, See FIGURE 7 | ±0.5 TYP | | | | nA |
| | | | | ±2.0 | | ±100 | |
| Drain off leakage | ID (Off) | VD = ±14 V, VS = ∓14 V, See FIGURE 7 | ±0.5 TYP | | | | |
| | | | | ±2.0 | | ±100 | |
| Channel on leakage | ID, IS (On) | VD = ±14 V, See FIGURE 8 | ±0.5 TYP | | | | |
| | | | | ±2.0 | | ±200 | |
| Digital inputs | | | | | | | |
| Input high voltage | VINH | | | | 2.4 | | V |
| Input low voltage | VINL | | | | | 0.8 | V |
| Input current | IINL, IINH | | | | | 1 | µA |
| Dynamic characteristics | | | | | | | |
| tOPEN | | See FIGURE 9 | 30 TYP | | | | ns |
| tON 3/ | | See FIGURE 9 | | 300 | | | |
| tOFF 3/ | | See FIGURE 9 | | 2650 | | | |
| Off isolation | | VS = 10 V p-p, f = 100 kHz, RL = 75 Ω, See FIGURE 11 | 80 TYP | | | | dB |
| Channel to channel crosstalk | | See FIGURE 12 | 80 TYP | | | | dB |
| CS (Off) | | | 5 TYP | | | | pF |
| CD (Off) | | | 5 TYP | | | | |
| CD, CS (On) | | | 16 TYP | | | | |
| CIN Digital input capacitance | | | 5 TYP | | | | |
| QINJ Charge injection | | RS = 0 Ω, CL = 1000 pF, VS = 0 V See FIGURE 10 | 20 TYP | | | | pC |

See footnote at end of table.

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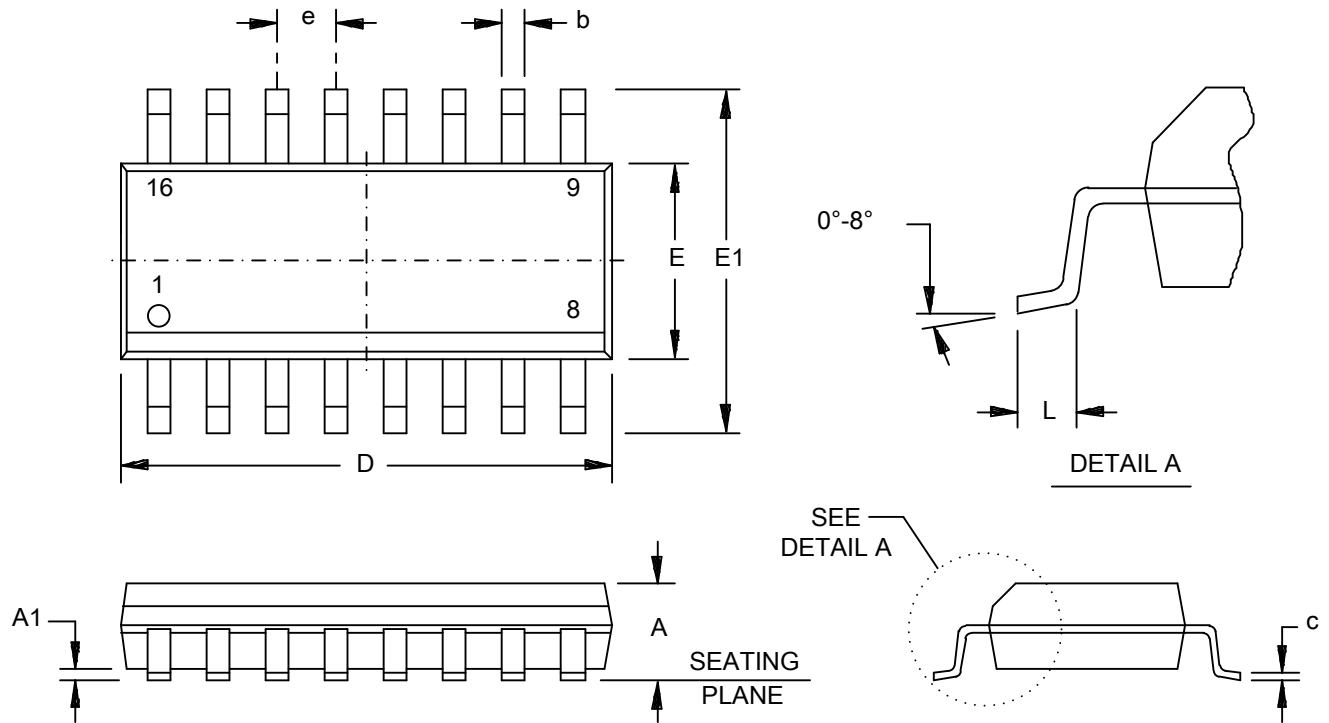
TABLE I. Electrical performance characteristics - Continued. 1/

| Test | Symbol | Test conditions <u>2/</u> | Limits | | | | Unit |
|---------------------------------|--------|---|---------|-----|----------------|-----|------|
| | | | 25°C | | -55°C to +125° | | |
| | | | Min | Max | Min | Max | |
| DUAL SUPPLY – Continued. | | | | | | | |
| Power supply | | | | | | | |
| I _{DD} | | Digital inputs = V _{INL} or V _{INH} | 0.6 TYP | | 2 | mA | |
| I _{SS} | | | 0.1 TYP | | 0.2 | | |
| Power dissipation | | | | | 33 | mW | |

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ V_{DD} = 15 V ±10%, V_{SS} = - 15 V ±10%, GND = 0 . All specifications -55°C to +125, unless otherwise noted.
- 3/ Sample tested at 25°C to ensure compliance.

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Case X



| Dimensions | | | | | | | | | |
|------------|-------------|-------|--------|------|--------|-------------|------|----------|------|
| Symbol | Millimeters | | Inches | | Symbol | Millimeters | | Inches | |
| | Min | Max | Min | Max | | Min | Max | Min | Max |
| A | 1.35 | 1.75 | .053 | .069 | E | 3.80 | 4.00 | .150 | .157 |
| A1 | 0.10 | 0.25 | .004 | .010 | E1 | 5.80 | 6.20 | .228 | .244 |
| b | 0.31 | 0.51 | .012 | .020 | e | 1.27 BSC | | .050 BSC | |
| c | 0.17 | 0.25 | .007 | .010 | L | 0.40 | 1.27 | .016 | .050 |
| D | 9.80 | 10.00 | .386 | .394 | | | | | |

NOTES:

- Controlling dimensions are in millimeters; inch dimensions are rounded-off millimeter equivalents for reference only and are not appropriate for use in design.
- Falls within JEDEC MS-012-AC.

FIGURE 1. Case outline.

| | | | |
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| Case outline X | | | |
|-----------------|-----------------|-----------------|-----------------|
| Terminal number | Terminal symbol | Terminal number | Terminal symbol |
| 1 | IN1 | 16 | IN2 |
| 2 | D1 | 15 | D2 |
| 3 | S1 | 14 | S2 |
| 4 | V _{SS} | 13 | V _{DD} |
| 5 | GND | 12 | NC |
| 6 | S4 | 11 | S3 |
| 7 | D4 | 10 | D3 |
| 8 | IN4 | 9 | IN3 |

NC = No Connect

FIGURE 2. Terminal connections.

| Case outline X | | |
|----------------|-----------------|---|
| Terminal | | Description |
| Number | Mnemonic | |
| 1 | IN1 | Logic control input. |
| 2 | D1 | Drain terminal. Can be an input or output. |
| 3 | S1 | Source terminal. Can be an input or output. |
| 4 | V _{SS} | Most negative power supply. This pin is used in dual supply applications only and should be tied to ground in single supply applications. |
| 5 | GND | Ground (0 V) reference. |
| 6 | S4 | Source terminal. Can be an input or output. |
| 7 | D4 | Drain terminal. Can be an input or output. |
| 8 | IN4 | Logic control input. |
| 9 | IN3 | Logic control input. |
| 10 | D3 | Drain terminal. Can be an input or output. |
| 11 | S3 | Source terminal. Can be an input or output. |
| 12 | NC | No connect. Not internally connected. |
| 13 | V _{DD} | Most positive power supply. |
| 14 | S2 | Source terminal. Can be an input or output. |
| 15 | D2 | Drain terminal. Can be an input or output. |
| 16 | IN2 | Logic control input. |

FIGURE 3. Terminal function.

| | | | |
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| Input INx | Switch condition |
|--------------|---------------------|
| 0 | On |
| 1 | Off |

FIGURE 4. Truth table

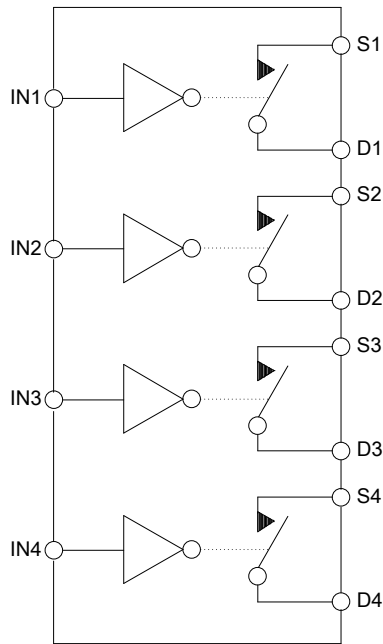


FIGURE 5. Functional block diagram.

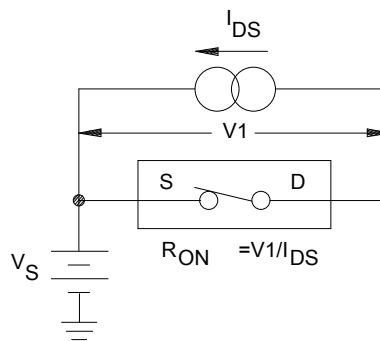


FIGURE 6. On resistance.

| | | | |
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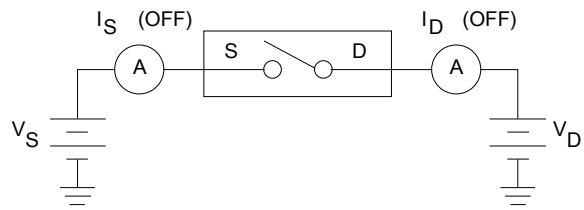


FIGURE 7. Off leakage.

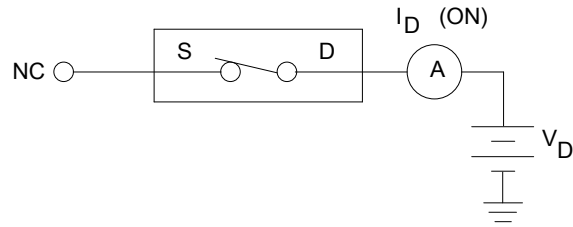


FIGURE 8. On leakage.

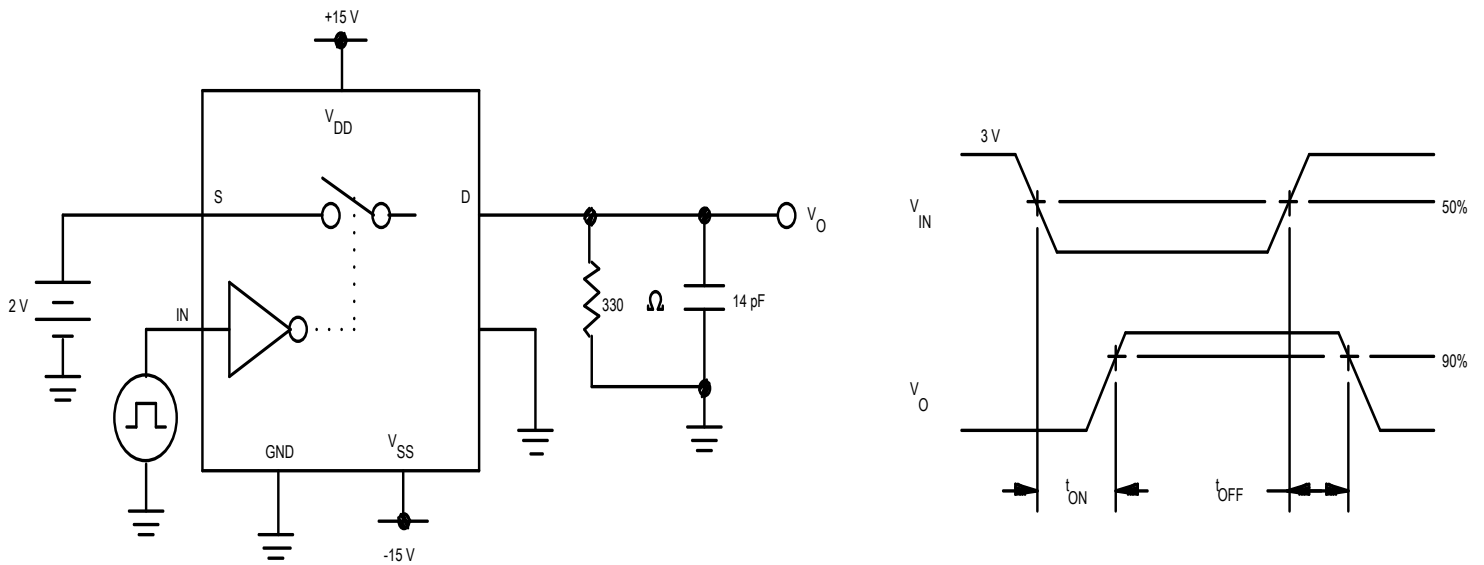


FIGURE 9. Switching time.

| | | | |
|---|---|---|--|
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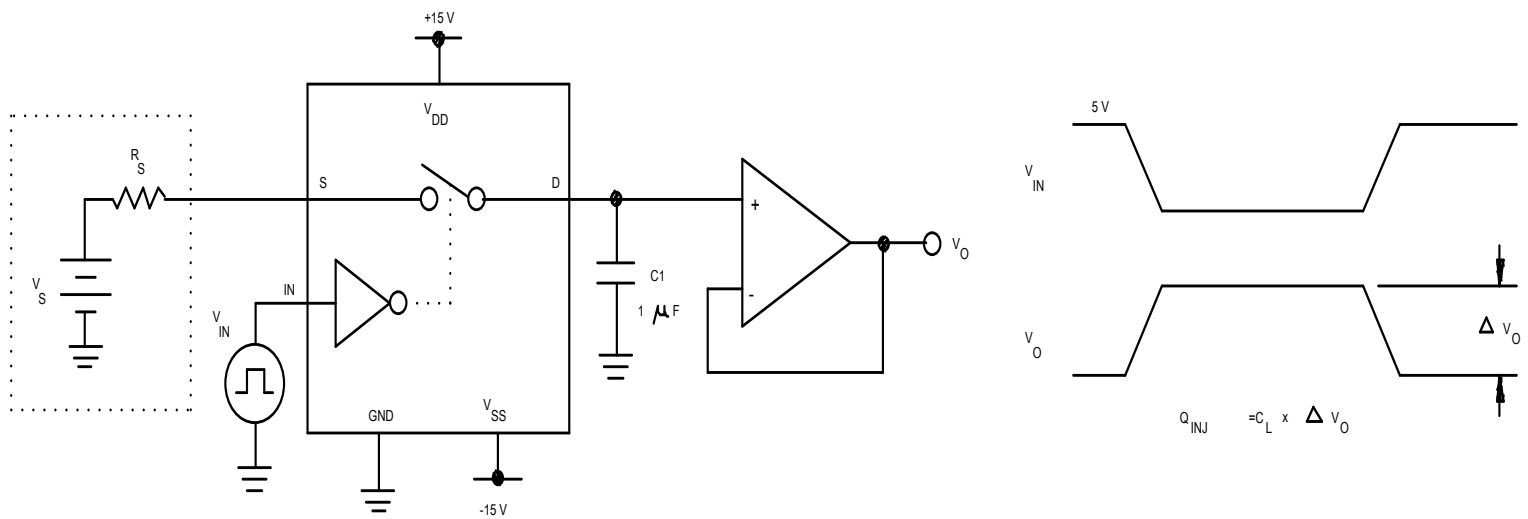


FIGURE 10. Charge injection.

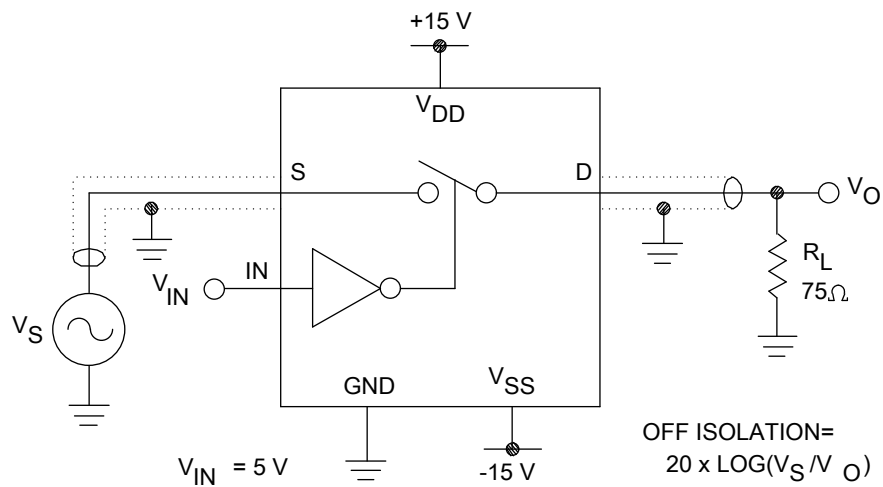


FIGURE 11. Off isolation.

| | | | |
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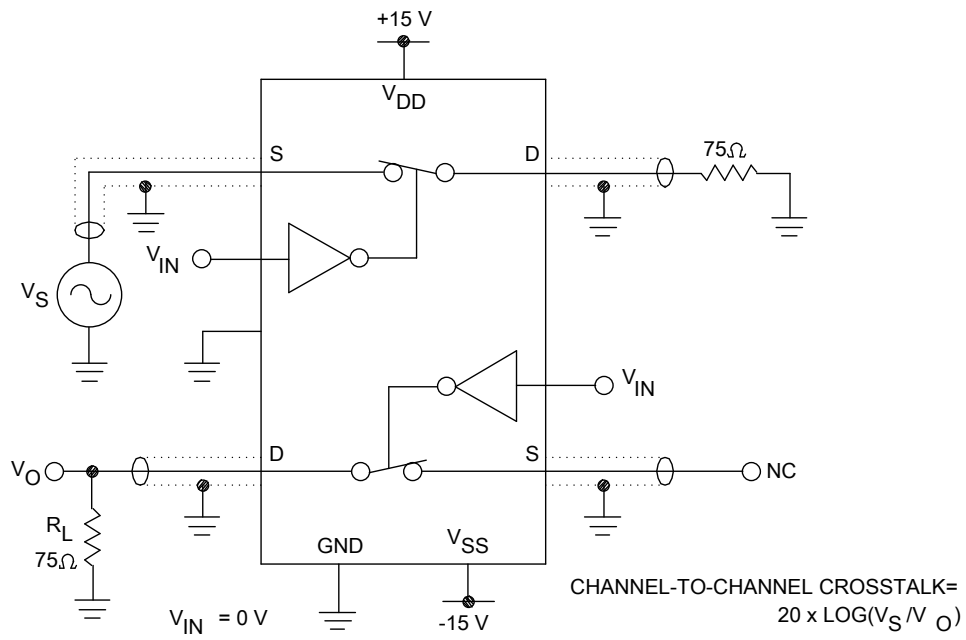


FIGURE 12. Channel to channel crosstalk.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

| | | |
|---|-------------------------------|--------------------|
| Vendor item drawing administrative control number <u>1/</u> | Device manufacturer CAGE code | Vendor part number |
| V62/12638-01XE | 24355 | ADG201ASRZ-EP-RL7 |

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
 1 Technology Way
 P.O. Box 9106
 Norwood, MA 02062-9106

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